Using Silicon-Germanium Mainstream BICMOS Technology for X-Band and LMDS (25-30 GHz) Microwave Applications

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ABSTRACT — **The 0.18μm SiGe HBT BICMOS technology we have developed has found a variety of uses in high-speed digital applications, up to 50 Gb/s [1]. This paper focuses on the use and applicability of this mainstream HBT BICMOS technology for microwave applications, particularly X-band, satellite, and LMDS (20-30 GHz). We will discuss the pros and cons relative to the well-known III-V MMIC technology, as well as Si microwave circuits on high-resistivity substrates (SIMMWICs [2]). It is shown that the SiGe BICMOS technology is widely applicable to microwave technology, with examples such as filters switches, and VCOs. We will also review new technology developments that can be applied to the SiGe BICMOS technology.**

I. INTRODUCTION

With the advent of volume applications in the X-band (radar, phased-array, beam-steering, etc) and LMDS bands (20-30 GHz microwave point-to-point transmission), a low-cost volume technology applicable to microwave circuits (MMICs) is required. Until now, high-performance III-V MMICs, with a semi-insulating substrate, have been the mainstay of these markets. SiGe HBT microwave ICs (SIMMWICs) have also been demonstrated on high-resistivity silicon substrates [2], with low levels of integration. If the performance were acceptable, use of a high-volume conventional silicon-based processing technology would help lower the cost and open up the application space.

Previously in our 50 GHz f_T SiGe HBT technology, we have shown how the addition of a thick polyimide/ metal layer has been used to realize X-band active and passive circuits [3]. Advancements in SiGe HBT technology, as well as the associated passive elements, have resulted in significant improvements in microwave performance even without the use of additional layers such as the polyimide described above.

The integration level of SiGe BICMOS, which allows low-power CMOS logic at <5 Gb/s to be integrated on the chip, allows for a variety of signal processing and conditioning to be done on chip. This allows a significant reduction in system chip count, power, and size.

II. TECHNOLOGY SUMMARY

The fabrication is based on a 0.18μm industry-standard CMOS with Cu-metallization. Process modules are added at various levels to fabricate a deep-trench isolated NPN SiGe HBT, using standard CMOS tooling. Additional process modules to fabricate microwave lumped elements such as resistors, varactors and MIM capacitors, as well as distributed elements such as transformers and transmission lines, are also added to the base process. Table I illustrates the range of devices available in this technology that make it suitable for microwave applications. The top metal layer (thick Al) is about 13μm from the silicon surface, reducing capacitive coupling and losses to levels previously achieved only with special processing [3,4].

TABLE I
Device Menu for 0.18μm SiGe HBT BICMOS

Device	
High-performance HBT	f_T=120 GHz, f_{MAX}=100 GHz(MAG), 120GHz (U)
High-Breakdown HBT	f_T=24 GHz, BV_{CBO}=10.0V BV_{CEO}=3.3V
High-performance nFET pFET	L_{EFF}=0.12μm, V_{DD}=1.8V L_{EFF}=0.14μm, V_{DD}=1.8V
High-voltage nFET pFET	L_{EFF}=0.29μm, V_{DD}=3.3V L_{EFF}=0.29μm, V_{DD}=3.3V
Metallization	Upto 5 levels Cu (0.4μm) 2 levels thick Al (4μm)
Poly-silicon resistors (Ω/sq) Thin-film resistor (above metal 1)	265 270 1600 140
Single crystal resistors (Ω/sq)	8 90
Decoupling capacitor (fF/μm^2)	2.6
Varactor (0-3V)	>3:1 tuning ratio
MIM capacitor (fF/μm^2)	1

Integration levels upto 150,000 HBTs or over 1 million CMOS transistors have been achieved in earlier generations of SiGe BICMOS, and the process described above is expected to yield similarly.

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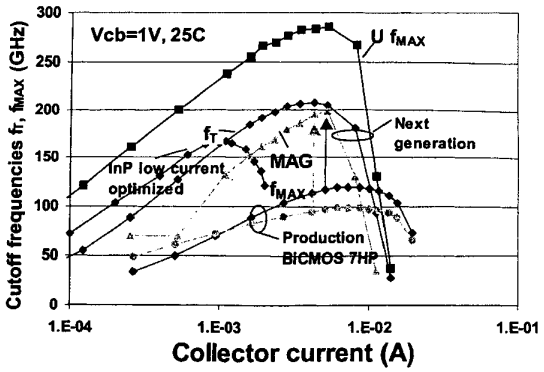

Fig. 1: f_T vs. collector current at V_{CB} = 1 V for generations of IBM SiGe NPN devices (InP shown for comparison).

III. ACTIVE DEVICES

A. NPN

Fig. 1 illustrates f_T vs. I_C for the latest 0.18 μm SiGe NPN compared against prior and future IBM SiGe generations as well as InP. The SiGe NPN transistor achieves high performance through vertical scaling of the epitaxially graded SiGe base and collector, leading to an f_T of 120 GHz. Simultaneously, lateral scaling combined with the use self-aligned collector and extrinsic base leads to improvements in f_{MAX} and power gain. SiGe continues to hold potential for yet greater speeds. Our next-generation SiGe NPN device have demonstrated f_T and f_{MAX}(U) values of 205/ 285 GHz, a record measurement for any silicon-based transistor and faster than competing InP-based devices tuned for similar low-power use.

Good noise performance is critical for microwave active device operation. The dominant noise contributor at low frequencies (<5 GHz) is R_B, which we reduce by maximizing emitter perimeter within the constraint of maintaining the high f_T needed for low noise at higher frequencies. At 10 GHz, with I_C = 8 mA, V_{CE} = 1.5 V, the a 25.6 μm^2 emitter area SiGe HBT achieves a value for F_{min} of less than 0.6 dB with 12.5 dB G_A. Aided by the high device f_T and low-C_{CB} (high f_{max}) layout, this F_{min} is 0.8 dB better than our prior 0.18 μm results (2 dB better than for 0.25 μm generation) and is within 0.2 dB of the performance of 0.2 μm AlGaAs/InGaAs PHEMTs for similar values of G_A (4). At 20 GHz, a band of particular interest for wireless local-loop applications (e.g. LMDS), F_{min} remains less than 1.8 dB, with a G_A of 7.5 dB.

The noise matching characteristics of the SiGe low noise NPN are shown in Fig. 2, plotting 1 and 2 dB noise contours on a polar chart. With a 10 GHz Γ_{opt} near the chart edge, the 51.2 μm^2 shows tight noise circles that avoid 50 Ω. In contrast, the 25.6 μm^2 contours are further from the chart edge and display a small R_n of 0.04, leading to relaxed circles that more closely approach the chart

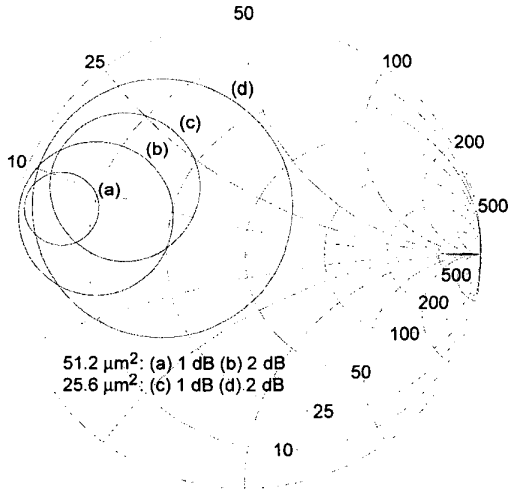

Fig. 2: 1 dB and 2 dB noise circles at 10 GHz for A_E = 0.2 x 6.4 μm^2, (0.2 x 4 μm^2) x 32 and (0.2 x 4 μm^2) x 64 SiGe NPN transistors, illustrating impact of scaling on 50 Ω performance.

center. The device sizes characterized here are drawn from those available on our test layout to illustrate the impact of emitter scaling on simple 50 Ω match. The transistors are presently not sized optimally for such a match at 10 GHz.

B. FETs

Because of digital scaling (the use of short channel length and thin gate oxide), the CMOS devices are also high performance. The nFET achieves a cutoff frequency of 85 GHz. The S-parameters of a multi-finger nFET from 1-40 GHz are shown in Fig. 3. Higher voltage 3.3V FET devices are also available for handling I/O functions or analog functions that require greater voltage headroom. The FETs can also be used for lower speed CMOS logic and interface functions, and for switching on and off various components & circuit blocks, resulting in lower

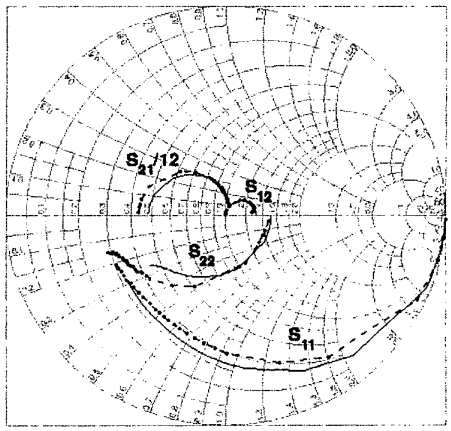

Fig. 3: nFET corrected S-parameters (0.1-40 GHz). W/L=10/0.18μm x 16 fingers, Vd=Vg=1.8V.

total system power.

IV. PASSIVE ELEMENTS

A. Lumped Element Passives

At 30 GHz, with a wavelength of 10 mm, it is not possible to use truly distributed components as the chip size would be prohibitive. Instead we used lumped passive elements. In order to improve component quality factors and reduce losses at microwave frequencies, we have moved the resistor and capacitor up into the metallization. The inductor and transmission lines were moved away from the substrate (with a thick low-loss silicon dioxide dielectric). A striped layout for the varactor is used to increase the Q.

Fig. 4 shows modeled resistor values as a function of frequency for a 50-ohm thin-film resistor above metal 1, showing good behaviour out to 30 GHz. Similarly good

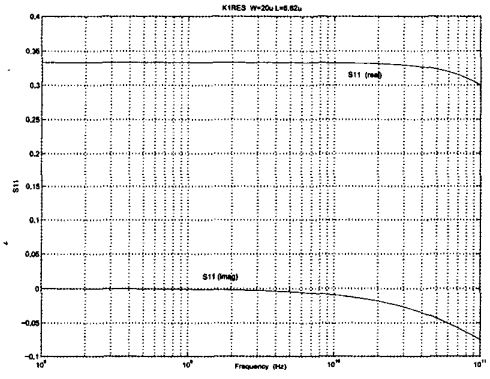

Fig. 4: Thin-film resistor characteristics (6.6x20 μm resistor with a value of about 50 ohms) as a function of freq.

high-frequency performance is shown by the MIM, which uses a thin silicon nitride dielectric, aluminum plates, and many via contacts to top and bottom plates. Using a stripe MIM with a high aspect ratio (W/L) will increase the useable frequency range.

B. Distributed Elements - Transmission Lines

Because multi-level metallization is common in (BI)CMOS, it can be used to create transmission lines. In a cross-section of typical III-V microstrip, the ground-plane is on the back of the (100 μm thick) semi-insulating substrate, compared to a multi-level metal microstrip with silicon dioxide dielectric (which has low loss at microwave frequencies). The losses (Fig. 5) for a microstrip near 50 ohms impedance are typically about 4-5 dB/cm at 20 GHz, compared to 1-1.5 dB/cm for III-V microstrip.

Because the separation of the ground-plane from the micro-strip is about 10μm, it is possible to put microstrip lines much closer together without much coupling. In addition, the effect of an inversion layer at the silicon surface is removed by using the first metal as the ground plane. As a result, it becomes possible to truly integrate microwave MMICs with many components on a small area chip. It should also be noted that chip sizes larger than 20x20mm (particularly with large area of passive components) should be very high yield in this silicon production technology.

V. APPLICATIONS

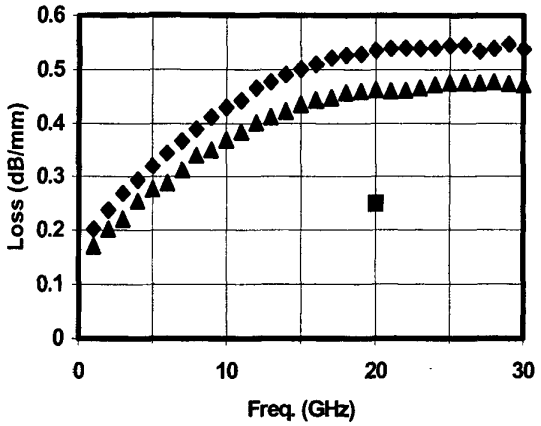

Fig. 5: Measured loss for a 1mm long, 5μm wide AM microstrip line (diamonds) and CPW line (triangles) (~50Ω) with M1 ground plane (oxide dielectric). The 20 GHz comparison point is 4μm Al line/ 8μm polyimide dielectric (sq.).

Digital ring-oscillator speeds down to 4.25 ps (fastest in any semiconductor technology) have been measured. Voltage-controlled oscillators with center frequencies up to 40 GHz have been fabricated in the production 0.18μm BICMOS technology. We describe below specific microwave applications.

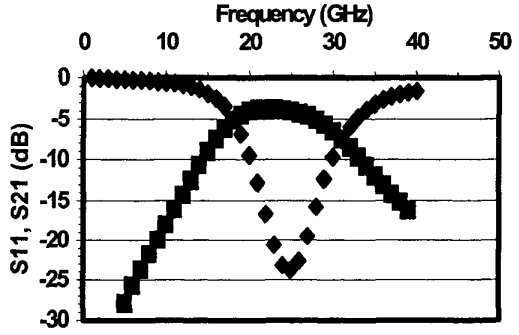

Fig. 6: Simulated Isolation and Insertion loss for a two-pole CPW filter with a pass-band at 25 GHz, in the standard proc. (BICMOS- 4μm thick Al last metal). Total size is 0.25 x 4 mm.

A. Band-pass Filter

The thick Aluminum last metal layer can be use to create CPW distributed-element filters. A two-pole band-pass filter is simulated as in [4] using an EM simulator which accounts for skin effect and achieves an insertion loss of 3.75 dB and isolation of 20 dB at 25 GHz pass-band (Fig. 6). Filters such as these would be useful in LMDS circuits.

B. Microwave Switch

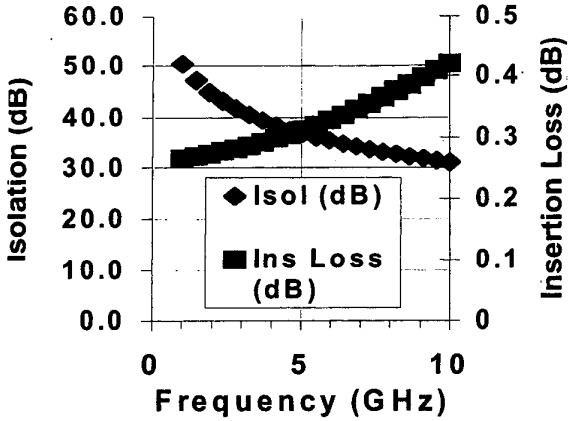

Fig. 7: Simulated small-signal isolation and insertion loss for a series-shunt nMOS switch (series FET 0.18x30μmx10 fingers, shunt nFET 0.18x10μmx10 fingers).

A series-shunt microwave FET switch is simulated using small-signal analysis, with the 0.18μm nMOSFETs available in the production BICMOS technology. The total gate-length in series and shunt legs has been separately optimized. Small-signal insertion loss of 1 dB and isolation of 20 dB are simulated at 10 GHz (X-band).

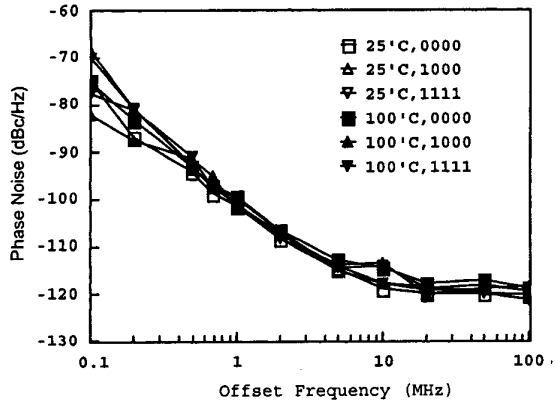

Fig. 8: 21.5 GHz VCO phase noise as a function of temperature and 4-bit coarse frequency control. The codes ('0000',..) represent digital capacitor selection.

These can be used as replacement for PIN diodes (used in earlier generations of SiGe BICMOS) in phase shifters [3].

C. VCO

With the bipolar, CMOS, varactor, and high Q inductor all available on the same chip, high frequency operation together with complex control functions may be implemented in the VCO. In particular, the CMOS logic and high FET performance has been used to advantage to implement a wide tuning range of 1.98GHz in a 21.5GHz VCO with a completely integrated tank circuit, exhibiting low phase noise across center frequency and temperature (Fig. 8) [1]. While this VCO was designed for low-jitter digital applications, similar VCOs can be designed for microwave transceivers.

VI. FUTURE ENHANCEMENTS

To reduce the substrate losses in silicon, a higher resistivity substrate can be used. The reduced losses are used to improve inductor Q and transmission line characteristics. Silicon substrate resistivity can also be locally increased using proton implantation into silicon. A transferred-substrate technology using wafer bonding [5] can be used to reduce parasitic substrate effects and reduce microwave losses even further. Addition of a thick metal-on-dielectric module can be used for lower loss transmission lines.

In summary, a 0.18μm production BICMOS technology has been characterized and it is shown that it is very useful for microwave applications such as X-band radar, satellite, or even LMDS at 25-30 GHz.

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